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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,167	11/07/2001	Richard H. Lane	M4065.0463/P463	4959

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EXAMINER	
BROPHY, JAMIE LYNN	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/986,167	LANE ET AL.	
	Examiner	Art Unit	
	J. L. Brophy	2822	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *22-38* is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-9,11-14,17-19 and 21* is/are rejected.

7)☒ Claim(s) *10,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 7/29/03.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (6,200,855) in view of Moise et al.

Lee teaches a method that comprises forming a pair of spaced word lines;

Forming source and drain regions on opposite sides of the word lines to define a plurality of memory cell access transistors 104 within a memory cell array area;

Forming a pair of access transistors 104 sharing a source/drain region;

Forming at least one first insulating layer 108 over the access transistors 104;

Forming a pair of capacitor polysilicon plugs 110b and a bit line polysilicon plug 110a through the first insulating layer 108 to the source and drain regions of the access transistors 104;

Forming at least one second insulating layer 126 over the polysilicon plugs 110a, 110b;

Forming container capacitors respectfully associated with each of the access transistors in the second insulating layer 126 over and in electrical communication with respective capacitor polysilicon plugs 110b;

Forming N-channel and P-channel peripheral logic transistors in a peripheral circuitry area;

Forming peripheral metal plugs 128a through the first 108 and second 126 insulating layer to contact the N-channel and P-channel peripheral logic transistors (col. 6, lines 53-58);

Forming at least one third insulating layer 131 over the container capacitors; and

Forming metal contacts 133 through the third insulating layer 131 to contact the peripheral metal plugs 128a.

See Figs. 2A-2D and accompanying text.

In addition, Lee teaches that excessive heat is released during the capacitor forming process. However, Lee does not specifically teach the step of heat treating the capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed.

Moise et al teach the step of heat treating a capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed (col. 10, lines 17-26).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Lee by performing a heat treatment on the capacitors because a person of ordinary skill in the art at the time the

invention was made would have been motivated to perform a heat treatment on the capacitors in order to crystallize the dielectric layer or control the stress in the electrodes (see Moise et al, col. 9, lines 45-52 and col. 10, lines 17-26 and 59-61).

Claims 1-5, 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (5,858,831) in view of Moise et al.

Sung teaches a method that comprises forming a pair of spaced word lines;

Forming source and drain regions 31 on opposite sides of the word lines to define a plurality of memory cell access transistors within a memory cell array area 60;

Forming a pair of access transistors sharing a source/drain region 31;

Forming at least one first insulating layer 29 over the access transistors;

Forming a pair of capacitor polysilicon plugs 33 and a bit line polysilicon plug 33 through the first insulating layer 29 to the source and drain regions 31 of the access transistors;

Forming at least one second insulating layer 34 over the polysilicon plugs 33;

Forming container capacitors respectfully associated with each of the access transistors in the second insulating layer 34 over and in electrical communication with respective capacitor polysilicon plugs 33 comprising the step of: depositing a conductive layer 37 within a capacitor container opening 36 to form a bottom layer, planarizing an upper surface of the capacitor containers to remove any conductive layer material on the upper surface, depositing a dielectric layer 38 over the substrate, depositing an upper capacitor plate 39 over the dielectric layer 38;

Forming N-channel and P-channel peripheral logic transistors in a peripheral circuitry area 50; and

Forming peripheral metal plugs 45, 46 through the first 29 and second 34 insulating layer to contact the N-channel and P-channel peripheral logic transistors.

See Figs. 10-20 and accompanying text.

However, Sung does not specifically teach the step of heat treating the capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed.

Moise et al teach the step of heat treating a capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed (col. 10, lines 17-26).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Sung by performing a heat treatment on the capacitors because a person of ordinary skill in the art at the time the invention was made would have been motivated to perform a heat treatment on the capacitors in order to crystallize the dielectric layer or control the stress in the electrodes (see Moise et al, col. 9, lines 45-52 and col. 10, lines 17-26 and 59-61).

Claims 1-5, 7-9, 11-14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al (5,893,734) in view of Moise et al.

Jeng et al teach a method that comprises forming a pair of spaced word lines;

Forming source and drain regions 19 on opposite sides of the word lines to define a plurality of memory cell access transistors within a memory cell array area 8;

Forming a pair of access transistors sharing a source/drain region 19;

Forming at least one first insulating layer 26 over the access transistors;

Forming a pair of capacitor polysilicon plugs 38' and a bit line polysilicon plug 38' (plugs 38' comprise N-type polysilicon – see col. 6, line 45 through col. 7, line 17) through the first insulating layer 26 to the source and drain regions 19 of the access transistors;

Forming at least one second insulating layer 54 over the polysilicon plugs 38';

Forming container capacitors respectfully associated with each of the access transistors in the second insulating layer 54 over and in electrical communication with respective capacitor polysilicon plugs 38';

Forming N-channel and P-channel peripheral logic transistors in a peripheral circuitry area 9 (col. 5, lines 5-15);

Forming peripheral metal plugs 58 through the second insulating layer 54 to contact the N-channel and P-channel peripheral logic transistors;

Forming at least one third insulating layer 60 over the container capacitors;

Forming a metal bit line contact 56 through the second insulating layer 54 to the bit line polysilicon plug 38' at the same time as the peripheral metal plugs 58 are formed; and

Forming metal contacts 62 through the third insulating layer 60 to the peripheral metal plugs 58 and the bit line contact 56, wherein the metal contacts 62 have a smaller diameter than the peripheral metal plugs 58 and the bit line contact 56.

See Figs. 10-20 and accompanying text.

However, Sung does not specifically teach the step of heat treating the capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed.

Moise et al teach the step of heat treating a capacitor, wherein the heat treatment may be performed prior to forming the upper electrode or after all portions of the capacitors are formed (col. 10, lines 17-26).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Sung by performing a heat treatment on the capacitors because a person of ordinary skill in the art at the time the invention was made would have been motivated to perform a heat treatment on the capacitors in order to crystallize the dielectric layer or control the stress in the electrodes (see Moise et al, col. 9, lines 45-52 and col. 10, lines 17-26 and 59-61).

Allowable Subject Matter

Claims 10, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 20 is allowed.

The following is an examiner's statement of reasons for allowance: none of the references of record teach all of the process limitations as claimed. Specifically, re claims 10, 15 and 16, none of the references teach a method wherein the first metal conductors have an oval top down cross-sectional shape, in combination with the other claim limitations. Re claim 20, none of the references teach a method that comprises forming a container capacitor in a second insulating film, annealing the capacitor, and then etching through the second insulating film to define a bit line opening, in combination with the other claim limitations.

Response to Arguments

Applicant's arguments filed 7/29/03 have been fully considered but they are not persuasive.

Regarding the 35 U.S.C. 103(a) rejection over Lee in view of Moise et al, applicant argues that Lee teaches forming a metal contact only to a p+ impurity region of a transistor in a core region of the device after capacitors have been formed. However, in an alternative embodiment, Lee teaches that the metal contact to the n+ impurity region may be formed by the same method that was used to form the metal contact to the p+ impurity region (see col. 6, lines 53-58). Therefore, applicant argument is not persuasive.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. L. Brophy whose telephone number is (703) 308-6182. The examiner can normally be reached on M-F (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

J.L.B.

jlb

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